CLAIMS

Amendments to the Claims:

1.   (Currently Amended) A system for mitigating line-edge roughness on a
semiconductor device, comprising:

        a monitoring component that monitors information associated with ~~at least one
critical dimension~~ an original distance of a photoresist and line-edge roughness on a
photoresist;

        a non-lithographic shrink component ~~that facilitates selectively mitigating line-
edge roughness on the photoresist via a non-lithographic shrink technique~~ comprising at
least one of a chemical component, a shrink enhancement component that shrinks a gate
channel, or a thermal component that applies heat to the photoresist to a point for causing
the photoresist to just enter a liquid phase to mitigate line-edge roughness, which in turn
increases a distance between gates and decreases a thickness of the photoresist layer; and

        a trim etch component that ~~facilitates selectively satisfying the at least one critical
dimension specification on the photoresist, the trim etch component etches away a critical
dimension specification deviation on the photoresist created by the non-lithographic
shrink component~~ is utilized to mitigate the increased distance between the gates by
removing excess resist material resulting from the non-lithographic component so as to
restore the original distance of the photoresist.

2.   (Cancelled).

3.   (Previously Presented) The system of claim 1, the monitoring component
comprising at least one of a scatterometry system and a Scanning Electron Microscopy
system.

4.   (Currently Amended) The system of claim 1, further comprising a processor that
processes data associated with the ~~at least one critical dimension~~ an original distance of a
photoresist and line-edge roughness on a photoresist.

5.   (Currently Amended) The system of claim 4, the processor comprising an artificial intelligence component that facilitates making inferences regarding mitigating line-edge roughness ~~and achieving the at least one critical dimension specification~~ on a photoresist and restoring an original distance of a photoresist.

6.   (Original) The system of claim 5, the artificial intelligence component comprising at least one of a support vector machine, a neural network, an expert system, a Bayesian belief network, fuzzy logic, and a data fusion engine.

7.   (Currently Amended) The system of claim 1, further comprising a memory component that stores data associated with mitigating line-edge roughness ~~and achieving the at least one critical dimension specification~~ on a photoresist and restoring an original distance of a photoresist.

8.   (Original) The system of claim 7, the memory component comprising at least one of volatile and non-volatile memory.

9.   (Cancelled)

10.   (Currently Amended) A method for mitigating line-edge roughness on a semiconductor device, comprising:
       determining whether line-edge roughness is extant on a patterned photoresist;
       employing a non-lithographic shrink technique ~~to selectively mitigate line-edge roughness on the photoresist~~ comprising at least one of a chemical technique, an expansion technique, a shrink enhancement technique that shrinks a gate channel, or a thermal technique to heat a photoresist to a point for causing the photoresist to just enter a liquid phase to mitigate line-edge roughness, which in turn increases a distance between gates and decrease a thickness of the photoresist layer; and
       employing a trim etch technique to ~~selectively compensate for any increase in critical dimension between lines on the photoresist caused by the non-lithographic shrink~~

~~technique~~ mitigate the increased distance between the gates by removing excess resist
material resulting from the non-lithographic component so as to restore an original
distance of the photoresist.

11.   (Previously presented) The method of claim 10, further comprising processing
information associated with photoresist line status.

12.   (Previously presented) The method of claim 10, further comprising making
inferences regarding photoresist line status.

13.   (Previously presented) The method of claim 10, further comprising storing
information associated with photoresist line status.

14.   (Previously presented) The method of claim 10, the presence of line-edge
roughness is determined *via* employing at least one of a scatterometry technique and
Scanning Electron Microscopy.

15.   (Cancelled)

16.   (Previously Presented) The method of claim 10, further comprising generating
feedback data that facilitates controlling at least one parameter associated with at least
one of line-edge roughness mitigation and critical dimension maintenance.

17.   (Currently Amended) A system for mitigating line-edge roughness on a
semiconductor device, comprising:

        means for determining critical dimensions and line-edge roughness on a
photoresist;

        means for employing a non-lithographic shrink technique ~~to selectively mitigate
line-edge roughness on the photoresist~~ comprising at least one of a chemical technique,
an expansion technique, a shrink enhancement technique that shrinks a gate channel, or a
thermal technique to heat a photoresist to a point for causing the photoresist to just enter a

liquid phase to mitigate line-edge roughness, which in turn increases a distance between gates and decreases a thickness of the photoresist layer; and

means for ~~selectively~~ removing excess resist material resulting from the non-lithographic shrink technique to ~~achieve a target critical dimension on~~ restore an original distance of the photoresist.

18.   (Original) The system of claim 17, further comprising means for monitoring photoresist line status.

19.   (Original) The system of claim 17, further comprising means for processing information associated with photoresist line status.

20.   (Original) The system of claim 17, further comprising means for storing information associated with photoresist line status.

21.   (Original) The system of claim 17, further comprising means for making inferences related to photoresist line status.

22.   (Previously Presented) The system of claim 17, the means for mitigating line-edge roughness comprising means for performing a non-lithographic technique.

23.   (Original) The system of claim 17, the means for trimming excess resist material comprising means for performing a trim etch.

24.   (Previously presented) The method of claim 10, the trim etch technique recaptures an original target critical dimension, the original target critical dimension extant on the photoresist before employing the non-lithographic shrink technique.